REMARKS

Amendments have been presented to claims 1, 4, 16, 17, 26 and 27. These amendments were not done to overcome any of the cited articles and support for these changes are found throughout the specification.

35 U.S.C. 112, second paragraph, rejections

In the Office Action claims 1-2, 15, 17, 26, and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

In claim 1 "unitfor" has been amended to "unit for." Also, "plurality of" has been deleted and "subsystems" was changed to "subsystem" to provide clear antecedent basis for singular references to "subsystem" in claim 2.

The Examiner stated that it is not clear what selective structure is intended by be recited by the use.of "selectively" in claim 15. The Applicants question the need for structure to be recited at all in this method claim. What is claimed is "selectively outputting headers..." It is not limited to any particular structure, but rather the action element of selectively outputting. Claims 17 and 35 include similar language. The Applicants assert that these claims are in proper format as presented.

The Examiner also stated that the use of "selected" in claim 26 is unclear. Although the Applicants believe that claim 26 was clear as previously presented, the Applicants have removed "selected" from the claim.

The Applicants assert that claims 1-2, 15, 17, 26, and 35 are in condition for allowance in view of the above reasons and amendments. Therefore, the Applicants respectfully request that the Examiner withdraw these rejections of these claims.

35 U.S.C. 102(e) rejection

In the Office Action claims 1-4, 6-9, 11-20, 22-29, and 31-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen. The Applicants traverse these rejections of these claims.

Amended claim 1, for example, reads:

> A memory unit for use in an integrated circuit (IC) comprising:
> an array of memory cells;
> a first data transfer interface coupled to the array of memory cells to provide a first access path for a processor and a subsystem of the IC to access said array of memory cells;
> a second data transfer interface coupled to the array of memory cells to provide a second access path for said processor to access said array of memory cells; and
> a controller coupled to the array of memory cells and the first and second data transfer interfaces to control said array of memory cells and said first and second data transfer interfaces to facilitate accesses of said memory unit by said processor and said subsystem.

In the Office Action it is stated that Chen column 20, lines 53-54 anticipate the first and second data transfer interfaces. The Office Action goes on to state that arbitration node of the memory remote cluster adapter (MRCA) in Chen, fig. 19a, "44", anticipates the controller of claim 1, for example. Both column 20, lines 53-54 and reference number 44 of fig. 19a refer to the MRCA. Therefore, the Applicants assume that the Examiner's position is that the MRCA anticipates the first data transfer interface, the second data transfer interface, and the controller. The Applicants respectfully disagree with this position.

Chen does not teach, discuss, or suggest providing first and second access paths for a processor as required by claim 1, for example. The MRCA access paths 58 are coupled to three node remote cluster adapters (NRCAs). Each path 58 from the MRCA to a particular NRCA consists of a fetch data path and a store data path, see Chen column 10, line 29. That is, a path 58 has one line to provide an NRCA access to the MRCA and another line to provide the MRCA access to the NRCA. This is not the same as the first and second access paths discussed in claim 1, which both provide the

processor access to the memory. In Chen any particular processor has only one access path to any particular memory.

Additionally, Chen does not teach, discuss, or suggest a first and a second data transfer interface as recited in claim 1, for example. Claim 1 requires that there be a first and a second data transfer interface that respectively provide for the first and second access paths to the array of memory cells. The MRCA, on the other hand, acts as one interface between the shared resources and the remote clusters and likewise provides one access path 54 to the memory. If one were to argue that a different arbitration node 44 of the arbitration node means acted as the first data transfer interface and the MRCA acted as the second data tranfer interface than these interfaces would provide memory access paths for different processors, unlike the interfaces of claim 1.

Of course there may be other reasons why Chen does not anticipate claim 1; however, the Applicants believe that the above stated reasons are more than sufficient. Therefore, the Applicants respectfully request that the Examiner withdraw this rejection claim 1.

Claims 2-4 and 6-7 depend from, and include the same limitations as, claim 1. Therefore, these claims are patentably distinct from Chen for at least the above reasons and the Applicants respectfully request that the Examiner withdraw this rejection of these claims.

Claim 8, for example, recites:

> In a memory unit of an integrated circuit (IC), a method of operation comprising:
> queuing first memory accesses of a processor and a subsystem of the IC in inbound queues of a first data transfer interface;
> queuing second memory accesses of the processor in an inbound queue of a second data transfer interface; sequencing said first and second memory accesses into a single sequence of memory accesses; and
> servicing said first and second memory accesses in accordance with their sequence order.

The Office Action states that queuing first memory accesses of a processor and subsystem in inbound queues of a first data transfer interface is met by the MRCA,

while queuing the second memory accesses of the processor in an inbound queue of a second data transfer interface is met by the input queue of the arbitration node 44 depicted in Fig. 14. The Applicants disagree with this position.

Chen does not teach, suggest, or discuss queuing first memory accesses of a processor in inbound queues of a first data transfer interface and queuing second memory accesses of the processor in an inbound queue of a second data transfer interface. While it is unclear which of the seventeen arbitration nodes 44 the Examiner believes represent the first and second data transfer interfaces, it is clear that no two of them are coupled to the same processor to provide respective inbound queues for the first and second memory accesses. In Chen, each of the arbitration nodes #1-16 are coupled to two processors. However, none of the processors are coupled to two arbitration nodes. Therefore, it is impossible for a first data transfer interface to provide an inbound queue for first memory accesses of a processor, while a second data transfer interface provides another inbound queue for second memory accesses of the processor.

Of course there may be other reasons why Chen does not anticipate claim 8; however, the Applicants believe that the above stated reasons are more than sufficient. Therefore, the Applicants respectfully request that the Examiner withdraw this rejection claim 8.

Claims 9 and 11-15 depend from, and include the same limitations as, claim 8 and are therefore patentably distinct from Chen for at least the same reasons as claim 8. The Applicants respectfully request that the Examiner withdraw this rejection of these claims.

Claim 16 as amended recites:

An integrated circuit comprising:
a processor;
a plurality of subsystems; and
a memory unit coupled to said processor and said subsystems having at least a first access path to facilitate access by said processor and said subsystems to access said memory unit and a second access path to facilitate access by said processor.

As discussed above, Chen does not teach, suggest, or discuss providing a processor with first and second access paths to a memory unit as required by claim 16, for example. Therefore, the Applicants respectfully request that the Examiner withdraw this rejection of this claim.

Claims 17-20 and 22-26 depend from, and include the same limitations as, claim 16 and are therefore patentably distinct from Chen for at least the same reasons as claim 16. The Applicants respectfully request that the Examiner withdraw this rejection of these claims.

Claim 27 recites:

> In an integrated circuit (IC), a method of operation comprising:
> a processor and a plurality of subsystems of the IC successively making first memory accesses of a memory unit of the IC via a first access path in turn;
> the processor also successively making second memory accesses to said memory unit via a second access path in parallel; and
> the memory unit servicing said first and second memory accesses made through said first and second access paths in parallel.

As discussed above, Chen does not teach, suggest, or discuss the processor making a first memory access via a first access path and a second memory access via a second access path. With respect to this claim, the Office Action states these elements are met by Col. 15, lines 52-59. However, this cited portion refers to mapping one memory access (i.e., a memory reference). It does not show a processor making a first and second memory access along respective access paths. Note, that the access paths 50 and 52 of Figure 10 come from different arbitration nodes (i.e., they are not access paths for a common processor). Because Chen does not teach, suggest, or discuss every element of claim 27, for example, an anticipation rejection based on Chen is inappropriate. Therefore, the Applicants respectfully request the Examiner withdraw this rejection of this claim.

Claims 28-29 and 31-35 depend from, and include the same limitations as, claim 27 and are therefore patentably distinct from Chen for at least the same reasons. The Applicants respectfully request that the Examiner withdraw this rejection of these claims.

35 U.S.C. 103(a) rejections

In the Office Action claims 5, 10, 21, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Agarwala. The Applicants traverse these rejections of these claims.

The Examiner relies on Agarwala to teach setting fixed priorities for transfer units. Even assuming this is true, and further assuming that the combination of Chen and Agarwala is proper, the combination still fails to suggest, teach, or discuss a processor capable of accessing a memory along a first and a second access path. Because claims 5, 10, 21, and 30 all include this or a similar element an obvious rejection based on Chen in view of Agarwala is improper. Therefore, the Applicants respectfully request that the Examiner withdraw this rejection of these claims.

Claim objections

In the Office Action claims 36-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

For the foregoing reasons regarding the patentability of the underlying base claims, the Applicants assert that claims 36-38 are also allowable. Therefore, the Applicants respectfully request that the Examiner withdraw this objection to these claims.

CONCLUSION

In view of the foregoing, the Applicant respectfully submits that claims 1-38 are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at (503) 796-2972.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
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